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Silicon-Based Current-Controlled Reconfigurable Magnetoresistance Logic Combined with Non-Volatile Memory

Zhaochu Luo, Xiaozhong Zhang, Chengyue Xiong, and Jiaojiao Chen*

Silicon-based complementary metal-oxide-semiconductor (CMOS) transistors have achieved great success. However, the traditional development pathway is approaching its fundamental limits. Magnetoelectronics logic, especially magnetic-field-based logic, shows promise for surpassing the development limits of CMOS logic and arouses profound attentions. Existing proposals of magnetic-field-based logic are based on exotic semiconductors and difficult for further technological implementation. Here, a kind of diode-assisted geometry-enhanced low-magnetic-field magnetoresistance (MR) mechanism is proposed. It couples p-n junction's nonlinear transport characteristic and Lorentz force by geometry, and shows extremely large low-magnetic-field MR (>120% at 0.15 T). Further, it is applied to experimentally demonstrate current-controlled reconfigurable magnetoresistance logic on the silicon platform at room temperature. This logic device could perform all four basic Boolean logic including AND, OR, NAND and NOR in one device. Combined with non-volatile magnetic memory, this logic architecture with unique magnetoelectric properties has the advantages of current-controlled reconfiguration, zero refresh consumption, instant-on performance and would bridge the processor-memory gap. Our findings would pave the way in silicon-based magnetoelectronics and offer a route to make a new kind of microprocessor with potential of high performance.

1. Introduction

Silicon-based complementary metal-oxide-semiconductor (CMOS) transistors have achieved great success and become the mainstream of integrated logic circuits. However, the traditional pathway to enhance computational performance and decrease cost by continuous miniaturization is approaching its fundamental limits.[1] Magnetoelectronics combining properties of spin and charge, derives novel multifunctional devices and has broad application prospects.[2] The recent emergence of logic devices based on magnetoelectronics,[3–7] especially magnetic-field-based semiconductor logic devices,[8,9] shows promise for surpassing the development limits of CMOS logic and arouses profound attentions.[10–12] Yet, existing magnetic-field-based semiconductor logic devices are based on the high-mobility exotic semiconductor materials and incompatible with current mainstream silicon-based information technology. These disadvantages make existing magnetic-field-based semiconductor logic devices impractical for industrial production in the near future.

Large magnetoresistance discovered in high-mobility (>70 000 cm^2 V^{-1} s^{-1}) non-magnetic semiconductors bridges electronics and magnetics, and offers reliable logic outputs of high signal-to-noise ratio in magnetic-field-based logic.[9] This kind of magnetic-field-based logic is based on the magneto-diode effect and gives the insight of magnetic-field-based logic in non-magnetic semiconductor. However, for silicon – the mainstream semiconductor of information technology, because of its meditate mobility (≈1 000 cm^2 V^{-1} s^{-1}) and meditate band gap (≈1.1 eV), the route to achieve silicon-based magnetoresistance logic parallel with the magnetic-field-based logic of non-magnetic semiconductors with high mobility and small band gap (0.17 eV) would bring the problems of low magnetoresistance and high work voltage. These problems make this router infeasible. Even though some discoveries of large magnetoresistance at room temperature in silicon are reported, magnetoresistance at low magnetic field remains small and the conditions to achieve large magnetoresistance are harsh for conventional device.[14–17] These problems hinder the application in silicon-based magnetic-field-based logic.

In this paper, we achieve large low-magnetic-field magnetoresistance in silicon at room temperature with a simple structure by coupling p-n junction's nonlinear transport characteristic and Lorentz force, and the magnitude of magnetoresistance at the same magnetic field (>120% at 0.15 T) is comparable with that in high-mobility non-magnetic semiconductor.[9] This large magnetoresistance could offer reliable logic outputs of high signal-to-noise ratio in silicon-based magnetoelectronics logic.

Further, to realize reconfigurable Boolean logic operations, unique magnetoelectric symmetry is necessary. Hence, we tune the structure of magnetoresistance device to achieve a

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kind of current-controlled reconfigurable magnetoresistance logic. This logic device could perform all four basic Boolean logic including AND, OR, NAND and NOR in one device by tuning the applied current. Combined with non-volatile magnetic memory, this logic architecture with unique magnetoelectric properties has the advantages of current-controlled reconfiguration, zero refresh consumption, instant-on performance and would bridge the processor-memory gap. Our logic architecture would help to offer a feasible route to achieve a new kind of microprocessor with higher computational efficiency, lower consumption, higher integration and self-healing function.[11–13]

2. Results and Discussion

2.1. Diode-Assisted Geometry-Enhanced Low-Magnetic-Field Magnetoresistance

The basic magnetoresistance device consisted of lightly phosphorus-doped (n-type) silicon and voltage-stabilization diodes (see Experiment section), and all experiment data were measured at room temperature. Four electrodes at the corners of bulk silicon were labeled as the 1st, 2nd, 3rd and 4th electrode, respectively. For the magnetoresistance device at circuit configuration A shown in **Figure 1**a, when the applied current I was small, voltage drop on the diode U_{diode}, i.e., potential difference between the 1st and 4th electrode was smaller than diode's critical voltage U_C so that the current flowing through the diode was negligible. The resistance R defined as V/I, was very low, where V was the voltage measured by voltage meter. This state was defined as low resistance state (LRS). When I was greater than a critical value I_C, $U_{diode} > U_C$ and the current would flow into bulk silicon from the 4th electrode through the diode. Hence, R increased rapidly, which was defined as high resistance state (HRS). Accompany with the resistance transition from LRS to HRS, an inflection point appeared in I-V curve shown in Figure 1b. When magnetic field B was applied perpendicularly to the device, the trajectory of electron was deflected due to Lorentz force. At the magnetic field of positive direction ($B > 0$) shown in Figure 1c, the equipotential line would rotate anticlockwisely. The potential difference of the 1st and 4th electrode increased and the critical applied current I_C, where the diode was switched, would decrease. Thus,

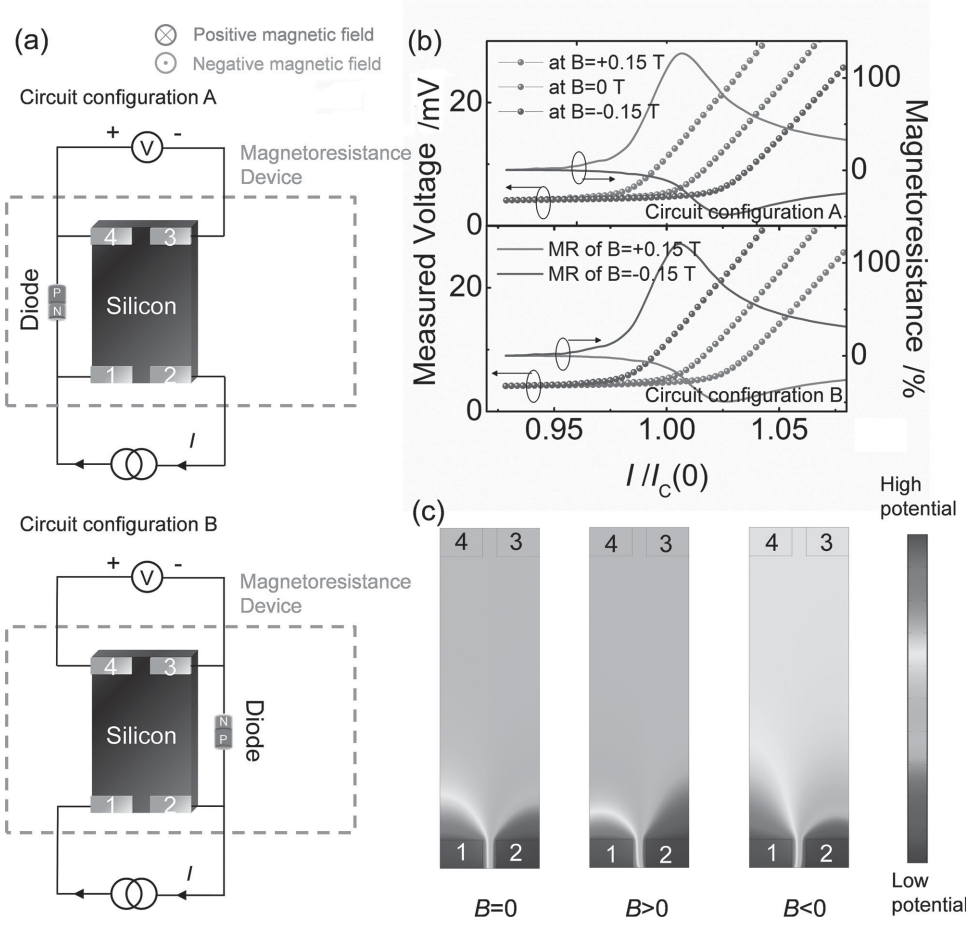

Figure 1. a) Schematics of magnetoresistance device at circuit configuration A and B. The magnetoresistance device consisted of voltage-stabilization diode and a rectangular silicon bulk with four titanium electrodes at corners. The arrows in circuit diagrams denoted directions of the current flow. b) I–V curves at circuit configuration A and B under different magnetic field and corresponding magnetoresistance distribution. The sign of magnetic field was defined in Figure 1a. $I_C(0)$ was the inflection current at $B = 0$. c) Voltage potential distribution under different magnetic field.

the inflection point of *I–V* curve would shift to a lower current value. The magnetoresistance was defined as $[R(B)\text{-}R(0)]/R(0)$, where $R(B)$ and $R(0)$ were the resistance at magnetic field B and zero, respectively. It would be enhanced between two inflection points and approached its maximum at the inflection current of $B = 0$ shown in Figure 1b. In our devices, we achieved the performance that the maximum of magnetoresistance at low magnetic field of 0.15 T was larger than 120%. It should be noticed that the voltage-stabilization diode used in this work was commercial one and its magnetic response was negligible (see Figure S1, Supporting Information). According to the symmetry of magnetic field, equipotential line would rotate clockwisely at the magnetic field of negative direction ($B < 0$) and the potential difference of the 1st and 4th electrode decreased and the critical applied current I_C, where the diode was switched, would increase. This would result in a higher shift of inflection point of *I-V* curve and a large negative magnetoresistance could be achieved. This current-controlled extremely large low-magnetic-field magnetoresistance could offer reliable logic outputs of high signal-to-noise ratio in magnetic-field-based logic. The reversal of the sign of magnetoresistance at the magnetic fields of opposite directions would make the magnetoresistance device be able to distinguish the direction of the magnetic field. Thus, the directions of magnetic field could be regarded as logic inputs in our magnetoresistance device.

When the circuit configuration was switched to circuit configuration B shown in Figure 1a, the voltage drop U_{diode}, which switched the diode, became the potential difference of the 2nd and 3rd electrode. According to the potential distribution of device shown in Figure 1c, the potential difference of the 2nd and 3rd electrode decreased at B > 0 and increased at B < 0, while the potential difference of the 1st and 4th electrode increased at B > 0 and decreased at B < 0. Hence, at circuit configuration B, the inflection point in *I–V* curve would shift to a higher value at $B > 0$ leading to a large negative magnetoresistance, while it would shift to a lower value at $B < 0$ leading to a large positive magnetoresistance. It was reverse with that at circuit configuration A shown in Figure 1b. This unique magnetoelectric symmetry was crucial for reconfigurable property.

This magnetoresistance value was closely related with electrode geometry and could be tuned easily by adjusting the geometrical ratio of *W/L*, where *W* and *L* is the distance of the 1st-4th electrode and 1st-2nd electrode, respectively. In experiment, we fabricated devices with fixed $L = 800$ μm and varied *W*. Magnetoelectric transport properties were measured and the relation of the maximum of magnetoresistance at 0.15 T and geometrical ratio of *W/L* at the circuit configuration A was shown in **Figure 2**a. The maximum of magnetoresistance increased almost exponentially with the geometrical ratio of *W/L*.

The value of maximum magnetoresistance MR_{max} phenomenally depended on two factors: i) the differential resistance difference between LRS and HRS and ii) the shift ratio of the inflection current at magnetic field *B*. It could be approximately depicted as:

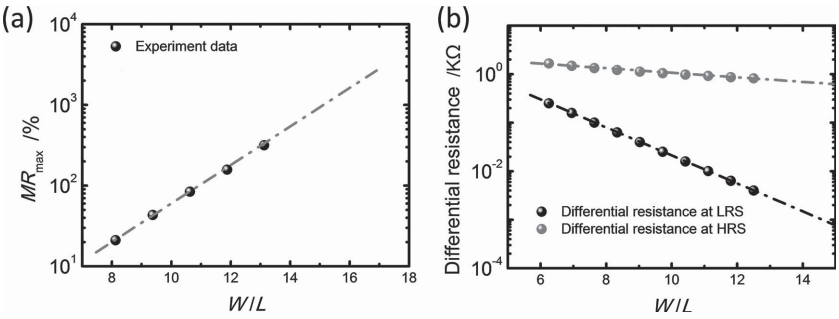

Figure 2. a) Relation between the maximum of magnetoresistance at $B = 0.15$ T and the geometrical ratio *W/L*. b) Relation between the differential resistance $\tilde{R}_{LRS}$, $\tilde{R}_{HRS}$ and the geometrical ratio *W/L*.

$$MR_{\max} \approx \frac{\tilde{R}_{HRS}}{\tilde{R}_{LRS}} \frac{I_C(0) - I_C(B)}{I_C(0)} \times 100\% \quad (1)$$

where $\tilde{R}_{LRS}$, $\tilde{R}_{HRS}$ and $I_C(B)$ were the differential resistance at LRS ($\tilde{R}_{LRS} = dV/dI$ at LRS), the differential resistance at HRS ($\tilde{R}_{HRS} = dV/dI$ at HRS) and the inflection current at magnetic field *B*, respectively. We could build a 2-D model by Finite Element Method (FEM) to help understanding this magnetoresistance mechanism. The geometry in the model was the same as the experiment devices and the equations were based on Laplace equation:

$$\nabla \cdot \left(\begin{bmatrix} \frac{\sigma}{1+\mu^2 B^2} & \frac{\mu B \sigma}{1+\mu^2 B^2} \\ \frac{-\mu B \sigma}{1+\mu^2 B^2} & \frac{\sigma}{1+\mu^2 B^2} \end{bmatrix} \cdot U \right) = 0 \quad (2)$$

where *U*, σ, μ and *B* was the voltage potential, silicon conductivity, silicon mobility and magnetic field, respectively. Applying suitable boundary conditions, electric transport characteristics under different magnetic fields could be obtained. According to the simulation results, the effect of geometry could be easily understood. Firstly, the voltage difference of the 3rd and 4th electrode decayed exponentially with increasing the *W/L* and the differential resistance at LRS was exponentially dependent on the *W/L*. However, the differential resistance at HRS was less sensitive to the *W/L*. Thus, the geometrical ratio could exponentially improve the resistance difference between LRS and HRS shown in Figure 2b. Secondly, according to the simulation results, the downward shift ratio of the inflection current increased slightly with the *W/L*. Therefore, the geometry with large *W/L* ratio provided i) large resistance contrast between LRS and HRS, leading to exponentially amplified MR and ii) more effective platform to reshape voltage distribution in wafers, leading to much improved low-field sensitivity of MR. Considering these two factors, the output ratio increased almost exponentially with the *W/L*, which was consisted with experiment results shown in Figure 2a.

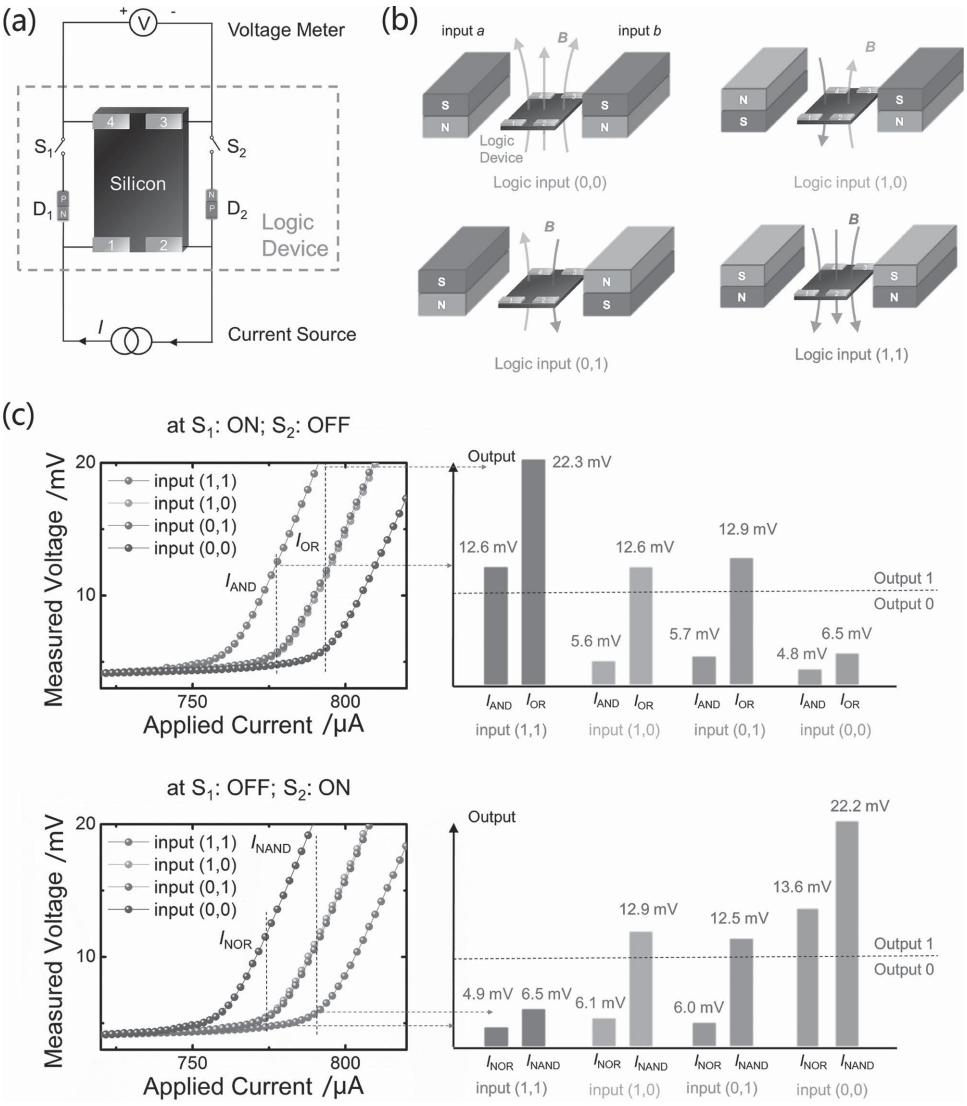

Figure 3. a) Schematics of logic device for one-device reconfigurable logic. b) Schematics of logic unit for one-device reconfigurable logic. Magnet's magnetization directions of down and up were defined as logic input 1 and 0, respectively. c) *I–V* curves at switch state of S_1: ON, S_2: OFF (up) and S_1: OFF, S_2: ON (down) for different logic inputs. Measured voltages not smaller and smaller than 10 mV were defined as logic output 1 and 0, respectively.

2.2. One-device Reconfigurable Boolean Logic

We have demonstrated a kind of diode-assisted geometry-enhanced low-magnetic-field magnetoresistance. This large low-magnetic-field magnetoresistance is attributed to both geometry of silicon and the diodes with rectifying effect. Then device structure symmetry should be elaborately modified to realize reconfigurable logic. Carefully considering all these parameters, we could fabricate a silicon-based current-controlled reconfigurable magnetoresistance logic device with good performance. Combined this silicon-based magnetoresistance device of unique magnetoelectric characteristics with magnets, one-device reconfigurable Boolean logic could be realized shown in **Figure 3**. Measured voltages at HRS and LRS were regarded as logic output 1 and 0, while magnet's magnetization directions of down and up were regarded as logic input 1 and 0, respectively. For the AND, OR, NOR and NAND logic operations, two logic inputs were required; so two magnets, which were regarded as two magnetic logic inputs, were placed around the device shown in Figure 3b. The logic input (*a*,*b*) denoted that logic inputs of left and right magnets were *a* and *b* (*a*,*b* = 1,0), respectively. Fringe field on the device would be tuned by switching magnets' magnetization directions and was ≈0.15 T when both magnetization directions were down (logic input (1,1)) (see Supporting Information Figure S2). When the left switch S_1 was ON (S_1: ON) and right switch S_2 was OFF (S_2: OFF), the logic device was degenerated into the circuit configuration A of magnetoresistance device and $I^{A}_{(0,0)} > I^{A}_{(1,0)} \approx I^{A}_{(0,1)} > I^{A}_{(1,1)}$, where $I^{X}_{(a,b)}$ was inflection point current for logic input (*a*,*b*) (*a*,*b* = 0,1) at circuit configuration *X* (*X* = A,B). In the range of $I^{A}_{(1,1)} \leq I \leq I^{A}_{(1,0)}$, the device for only logic input (1,1) was at HRS (logic output = 1), and for the other logic inputs of (0,0), (1,0), and (0,1) was at LRS (logic output = 0), which represented

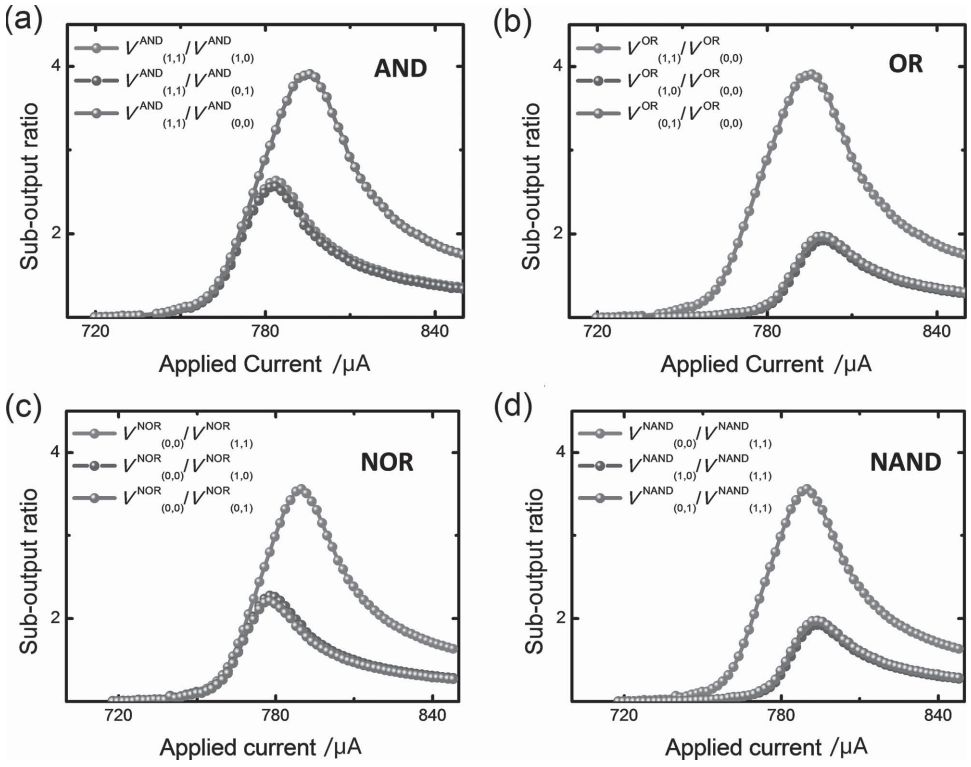

Figure 4. a) Sub-output ratios distribution for the AND logic operation. b) Sub-output ratios distribution for the OR logic operation. c) Sub-output ratios distribution for the NOR logic operation. d) Sub-output ratios distribution for the NAND logic operation.

the AND logic operation. In the range of $I^{A}_{(1,0)} \leq I \leq I^{A}_{(0,0)}$, the device for only logic input (0,0) was at LRS (logic output = 0), and for the other logic inputs of (1,1), (1,0), and (0,1) was at HRS (logic output = 1), which represented the OR logic operation.

Applied currents should be selected for the AND and OR logic operations in the range of $I^{A}_{(1,1)} \leq I \leq I^{A}_{(1,0)}$ and $I^{A}_{(1,0)} \leq I \leq I^{A}_{(0,0)}$ to get the highest output ratio, i.e., the highest ratio of output voltages between logic output 1 and 0. We began with the AND logic operation at circuit configuration A. In the range of $I^{A}_{(1,1)} \leq I \leq I^{A}_{(1,0)}$, the device for only logic input (1,1) was at HRS (logic output = 1) and for the other logic inputs was at LRS (logic output = 0). There were three kinds of output ratio values defined as sub-output ratios, i.e., $V^{AND}_{(1,1)}/V^{AND}_{(1,0)}$, $V^{AND}_{(1,1)}/V^{AND}_{(0,1)}$ and $V^{AND}_{(1,1)}/V^{AND}_{(0,0)}$, where $V^{X}_{(a,b)}$ represented the voltage for the X (X = AND, OR, NAND and NOR) logic operation and for logic input (a,b) (a,b = 1,0). We defined output ratio of AND logic operation as the minimum of these three sub-output ratios, i.e., $\min\{V^{AND}_{(1,1)}/V^{AND}_{(1,0)}, V^{AND}_{(1,1)}/V^{AND}_{(0,1)}, V^{AND}_{(1,1)}/V^{AND}_{(0,0)}\}$. The applied current was chosen to make the output ratio maximum. According to **Figure 4**a, the output ratio achieved the maximum at $I = I^{A}_{(1,0)}$ and this value was selected as I_{AND} for the AND logic operation. In the current range of the OR logic operation ($I^{A}_{(1,0)} \leq I \leq I^{A}_{(0,0)}$), there were also three sub-output ratios, i.e., $V^{OR}_{(1,1)}/V^{OR}_{(0,0)}$, $V^{OR}_{(1,0)}/V^{OR}_{(0,0)}$, and $V^{OR}_{(0,1)}/V^{OR}_{(0,0)}$, and we also defined output ratio of the OR logic operation was the minimum of these three sub-output ratios, i.e., $\min\{V^{OR}_{(1,1)}/V^{OR}_{(0,0)}, V^{OR}_{(1,0)}/V^{OR}_{(0,0)}, V^{OR}_{(0,1)}/V^{OR}_{(0,0)}\}$. According to Figure 4b, the output ratio achieved the maximum at $I = I^{A}_{(0,0)}$ and this value was selected as I_{OR} for the OR logic operation. Therefore, $I = I_{AND} = I^{A}_{(1,0)}$ ($I = I_{OR} = I^{A}_{(0,0)}$) was selected for the AND (OR) logic operation and the truth table with experiment results was summarized in **Table 1**.

For the NAND (NOR) logic operation, the relation of logic inputs and outputs was reverse compared with the AND (OR) logic operation. Hence, S_1: OFF and S_2: ON were adopted and the logic device was degenerated into circuit configuration B of the magnetoresistance device which had reversal relation of the magnetoresistance sign and magnetic field direction with circuit configuration A shown in Figure 3c. The relation of logic inputs and logic outputs in the range of $I^{B}_{(1,0)} \leq I \leq I^{B}_{(1,1)}$ and $I^{B}_{(0,0)} \leq I \leq I^{B}_{(1,0)}$ satisfied the logic operations of NAND and NOR, respectively. Similarly, $I = I_{NAND} = I^{B}_{(1,1)}$ ($I = I_{NOR} = I^{B}_{(1,0)}$) was selected for the NAND (NOR) logic operation to get the highest output ratio shown in Figure 4c and 4d, and the truth table with

Table 1. Truth table of the AND, OR, NAND and NOR logic operations in one-device reconfigurable Boolean logic.

Logic Input		Logic Output (Measured Voltage)			
		S_1: ON; S_2: OFF		S_1: OFF; S_2: ON	
a	*b*	*I* = 777 μA	*I* = 795 μA	*I* = 778 μA	*I* = 794 μA
1	1	1 (12.6 mV)	1 (22.3 mV)	0 (4.9 mV)	0 (6.5 mV)
1	0	0 (5.6 mV)	1 (12.6 mV)	0 (6.1 mV)	1 (12.9 mV)
0	1	0 (5.7 mV)	1 (12.9 mV)	0 (6.0 mV)	1 (12.5 mV)
0	0	0 (4.8 mV)	0 (6.5 mV)	1 (13.6 mV)	1 (22.2 mV)
		AND	**OR**	**NOR**	**NAND**

experiment results was summarized in Table 1. Therefore, the four basic logic operations of AND, OR, NAND and NOR could be transformed by controlling ON/OFF states of two switches and tuning applied current in one device. This was the so-called one-device reconfigurable magnetoresistance logic. Then the duplicate test for the one-device reconfigurable logic mode was conducted to demonstrate reproducibility and stability of output signals of the logic devices. The applied currents of different logic operations were selected and different logic inputs were switched manually with the order of (1,1), (1,0), (0,1), and (0,0). With the duplicate test of 140 times switches, the logic devices are reproducible and have stable performance of different logic operations.

Compared with traditional CMOS logic, one-device current-controlled reconfigurable property of our logic device makes processor higher computational efficiency per logic device. Furthermore, it could help to build a processor with self-healing function. If some logic devices failed, the rest logic devices in processor could be reconfigured by software to balance tasks without hardware-level modulation.[11,12]

2.3. Magnetic Random Access Logic

When one logic device was placed around one magnet to compose a logic unit, direct reconfigurable logic operations between two bits stored in two space-separated magnets could be realized shown in **Figure 5**a. In experiment, the distance between two logic units was large enough that the interaction of magnets in different logic units was negligible and fringe field on the logic device was only from the magnet of its logic unit. The distance between the logic device and its magnet was 4.5 mm and magnitude of fringe field on logic device was ~0.15 T (see Supporting Information Figure S3). I_i and V_i were the applied current and measured voltage of logic unit i (i = 1, 2), respectively. The output voltage V_{out} was equal to the addition of V_1 and V_2, which could be done by an adder. Logic input (a,b) (a,b = 0,1) represented the logic input state that logic input of logic unit 1 was equal to a and logic input of logic unit 2 was equal to b, respectively. Experiment data for different logic inputs were shown in Figure 5b to 5i. The definition of logic input was the same as that of one-device logic. Compared with 10 mV of one–device reconfigurable Boolean logic, the critical value separating logic output 1 and 0 was set as 20 mV. For the AND logic operation, logic output of only logic input (1,1) was 1, while logic outputs of the other logic inputs of (1,0), (0,1) and (0,0) were 0. Thus output voltage of only logic input (1,1) would be ≥20 mV, while output voltages of the other logic inputs would be <20 mV. Magnetoelectric transport characteristic at S_{11}: ON, S_{12}: OFF, S_{21}: ON and S_{22}: OFF could satisfy this logic relations and the area in I_1-I_2 plane where output voltage-logic input relation of the AND logic operation was satisfied, was shown in Figure 5b. Similarly, for the OR logic operation, logic output of only logic input (0,0) was 0, while logic outputs of the other logic inputs of (1,0), (0,1) and (1,1) were 1. Thus output voltage of only logic input (0,0) would be <20 mV, while output voltages of the other logic inputs would be ≥20 mV. Magnetoelectric transport characteristics at the switch state the same as the AND logic operation could satisfy its logic relations and the satisfied area was shown in Figure 5b. For the NAND (NOR) logic operations, the logic relations were reversal with that of the AND (OR) logic operation. Magnetoelectric transport characteristic at S_{11}: OFF, S_{12}: ON, S_{21}: OFF and S_{22}: ON could satisfy their logic relations according to the magnetoelectric symmetry of device. The areas in I_1-I_2 plane where output voltage-logic input relation of the NAND and NOR logic operation were satisfied, were shown in Figure 5f, respectively.

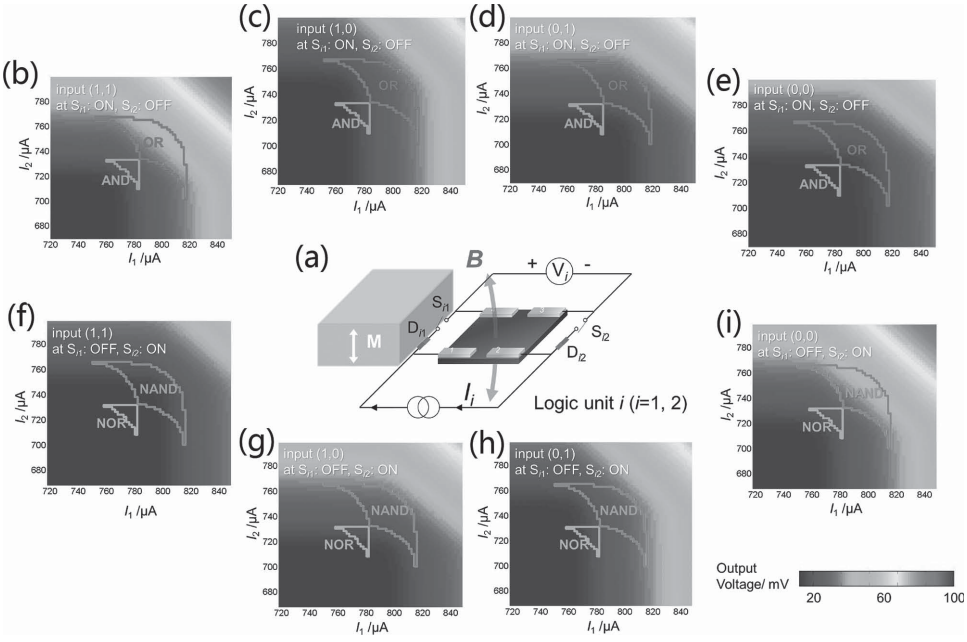

Figure 5. a) Circuit schematics of logic unit i (i = 1,2). b–i) Experiment data of I_1-I_2-V_{out} for different logic inputs at different switch states. The definitions of logic input 0 and 1 were the same as that for one-device reconfigurable Boolean logic. The areas in I_1-I_2 plane indicated by AND, OR, NOR and NAND satisfied the AND, OR, NOR, and NAND logic operations, respectively.

Table 2. Truth table of the AND, OR, NAND and NOR logic operations in magnetic random access logic.

Logic Input		Logic Output (Measured Voltage)			
		S_{11}: ON, S_{12}: OFF; S_{21}: ON, S_{22}: OFF		S_{11}: OFF, S_{12}: ON; S_{21}: OFF, S_{22}: ON	
a	*b*	I_1 = 779 μA, I_2 = 721 μA	I_1 = 795 μA, I_2 = 736 μA	I_1 = 778 μA, I_2 = 720 μA	I_1 = 794 μA, I_2 = 736 μA
1	1	1 (28.5 mV)	1 (45.9 mV)	0 (11.0 mV)	0 (15.2 mV)
1	0	0 (19.7 mV)	1 (30.3 mV)	0 (19.7 mV)	1 (33.5 mV)
0	1	0 (19.8 mV)	1 (30.1 mV)	0 (19.8 mV)	1 (33.2 mV)
0	0	0 (11.1 mV)	0 (14.6 mV)	1 (28.5 mV)	1 (47.1 mV)
		AND	**OR**	**NOR**	**NAND**

Further, we selected suitable applied current of I_1 and I_2 to get the highest output ratio with the method same as that of one-device reconfigurable logic and the truth table of these four logic operations was shown in **Table 2**.

Direct reconfigurable logic operations between two bits stored respectively in two space-separated magnets have been experimentally demonstrated. Further, if extending these logic operation modes to a non-volatile magnetic random access memory (MRAM) network, i.e., placing one logic device around every magnetic storage bit, Boolean logic operations between any two bits could be executed directly by tuning circuit configuration and applied current. Thus, we could extend this logic operation mode to magnetic random access memory and form a new kind of processor-memory architecture, which could be named after magnetic random access logic (MRAL). One logic device was placed around/below every nanomagnet and silicon-based controlling circuits could be fabricated around it on the same chip shown in **Figure 6**a. With this kind of processor-memory architecture, information bits could directly be operated without redundant transfer between memory and processor in traditional computer structure. Program instructions stored in nanomagnets were read to configure the controlling circuit. Then the controlling circuit would select two target bits, applied currents and switch states, and logic operation between these two bits would be directly executed. The logic operation result could be written into another nanomagnet. This result could be the data of next operation or program instructions for configuring the controlling circuit of next operation. These three processes composed one logic-memory process in MRAL shown in Figure 6b. This kind of logic-memory process needn't data/program instructions transfer through external memory and internal operation circuit, and had almost no delay between data read and logic operation, so it could bridge the processor-memory gap. Because of combining with non-volatile magnetic memory, the data and program instructions at run time were stored, and after powered off, the computer with this processor-memory architecture could be instant on. Moreover, with this simple, highly parallel structure, this kind of processor-memory architecture could allow the software to determine and implement the best resource allocation for each application, which implemented only a minimal set of mechanisms in hardware-level.[18] This operation mode has large degrees of freedom and would make computer flexible to do complex or unexpected work.

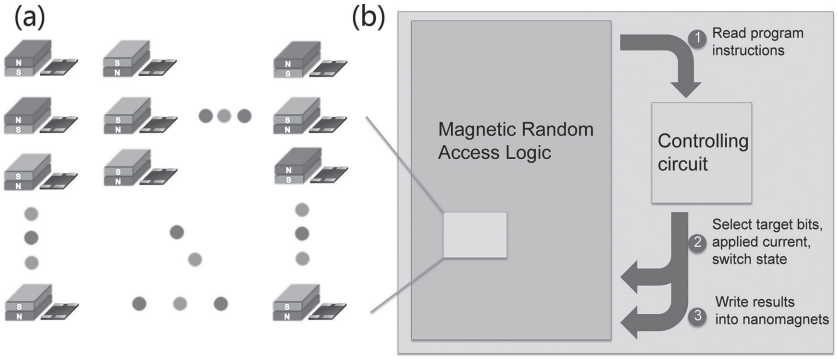

Figure 6. a) Structure schematics of magnetic random access logic. One nanomagnet was deposited around/above the logic device. b) Structure schematics of microprocessor with magnetic random access logic. One logic-memory process in this microprocessor included three sub-processes: 1) read program instructions in magnetic random access logic; 2) select target bits, applied current and switch state by controlling circuit; 3) write results into nanomagnets in magnetic random access logic.

2.4. Discussion of Integration

We have demonstrated the performance of current-controlled reconfigurable magnetoresistance logic combined with non-volatile memory in several logic units, but billions of logic units should be fabricated to compose one microprocessor. Thus, one key issue is the integration of large amount of logic units. Firstly, benefit from mature silicon-based technology, silicon-based logic devices could be easily miniaturized and integrated with low cost. The size of diode could be nanoscale for heavily doped silicon.[19] The critical factor which limits the miniaturization of silicon-based device is the work voltage and high work voltage may cause breakdown. If scarifying some output ratio, we could use diodes of low U_C such as forward p-n junction diode (U_C = 0.7 V) and Schottky diode (U_C = 0.3 V) to decrease the work voltage (see Figure S4 and S5, Supporting Information). Breakdown field of silicon is $\approx 3 \times 10^5$ V cm^{-1}[19] and the shortest distance between two electrodes could be scaled down into <100 nm with the forward p-n junction diode. Besides, ballistic transport appeared in nanoscale would increase breakdown field, which allowed continuous miniaturization.[20] Hence, the scaling down of our logic device doesn't have the physical

channel length limit of dead space which hinders the miniaturization of magneto-diode logic device.[9]

Secondly, patterned nanomagnet, which would be regarded as magnetic inputs, could be fabricated around/above silicon-based devices. The magnitude of fringe field on the logic device could reach hundreds of mT, depending on the geometry configuration of nanomagnet.[9] Magnetization direction of nanomagnet could be flipped by magnetic field generated by nanoscale electromagnetic coil or spin transfer toque (STT) effect.[21] Because the magnetic field on logic device is perpendicular to silicon wafer, our magnetic logic is compatible with perpendicular magnetic anisotropic (PMA) system, which has high thermal stability and low critical current for STT switching. For the integration of magnets, the crosstalk between different magnets from nearby logic units is a problem to limit the upper bound of the density of integration. According to our simulation of magnetic field distribution of magnets array, when the magnets were scaling down into 100 nm and the magnets distance was ≈400 nm, the overlapped stray field on the logic device of all magnets in other logic units would be negligible. Then, we could estimate that when the logic unit size is 100 nm, the density of integration would be 2.6 Gbit inch^{-2}. Moreover, materials with high permeability can be used as magnetic shields to attenuate interference magnetic field by several orders of magnitude.[22] This technique has commonly used in magnetic heads of hard disks to increase the density of data storage. If the magnetic shielding technology is applied in our logic system, the distance of logic units could be reduced and the density of integration would be further increased.

Further, we estimate the Joule dissipation of our device with the size of 100 nm would be <2 aJ for 1 ns pulse duration and this value is about three orders of magnitude smaller than that of current semiconductor-based logic devices (≈3.6 fJ) at same device size.[9] This low Joule dissipation would decrease the power density down to <20 W cm^{-2}, which is much lower than that of current semiconductor-based logic devices (≈1.8×10^4 W cm^{-2}) and even lower than that of nowadays CMOS logic device (≈100 W cm^{-2}).[23] Hence, our logic device could avoid the cooling problem in microprocessor chips. Moreover, theoretical magnetization switch consumption could be as low as the magnitude of aJ. Therefore, our device has the potential to be scaled down into nanoscale and integrated with ultralow consumption of aJ per logic operation. This energy consumption per logic operation is much lower than that of nowadays CMOS logic device (≈10^4 aJ).[24]

3. Conclusion

In summary, we propose diode-assisted geometry-enhanced low-magnetic-field magnetoresistance mechanism and achieve extremely large magnetoresistance of >120% in silicon with 0.15 T magnetic field at room temperature. With this magnetoresistance mechanism, silicon-based logic device of unique magnetoelectric symmetry is fabricated. Combined with magnets regarded as the source of magnetic field, this logic device could realize all four basic Boolean logic of AND, OR, NAND, and NOR in one device. Based on this logic device, a kind of processor-memory architecture named as magnetic random access logic is proposed. This logic architecture with unique magnetoelectric properties has the advantages of current-controlled reconfiguration, zero refresh consumption, instant-on performance and would bridge the processor-memory gap. Our work would help to build a high performance microprocessor and make silicon family further advanced.

4. Experimental Section

N-type silicon wafer was used for fabricating our logic device. It was (100) orientated and had the thickness of 500 μm. The resistivity and mobility were ≈3 000 Ohm cm and 1 200 cm^2 V^{-1} s^{-1}, respectively. Patterned Ti electrodes were deposited by pulsed laser deposition (PLD) to form Ohmic contacts and the electrode size was 1.5 mm × 1 mm. The distance of the 1st–2nd electrode was 800 μm and the distance of the 1st–4th electrode was 6–10 mm. Keithly 2400 and keithly 2182 were used as current source and voltage meter in our experiment. The magnet used in experiment was NdFeB magnet and the size was 25.4 mm × 12.7 mm × 6.35 mm. For one-device reconfigurable Boolean logic operations, two magnets were placed parallel at distance of 18 mm shown in Figure S2, Supporting Information. The logic device was placed in the center between two magnets and the magnetic field magnitude on it for logic input (1,1) was ≈0.15 T. For logic operations between two separated bits, one magnet was used and logic device was placed at distance of ≈4 mm away from magnet shown in Figure S3, Supporting Information. The magnetic field magnitude on the device was ≈0.15 T.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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